www.astri.org | From **Minds** to **Markets**

Next Generation Secure Portable Storage

Alan Cheung
R&D Director
Integrated Circuit Design Group

ASTRI™

香港應用科技研究院有限公司
Hong Kong Applied Science and Technology Research Institute Company Limited

Agenda

- Company Introduction
- IC Design Group, Applied SoC Design Team
- USB 3.0 Application Processor
- The Design of U3AP
- ASTRI Storage Design Platform
- Q&A

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Company Introduction

香港應用科技研究院有限公司
Hong Kong Applied Science and Technology Research Institute Company Limited

About ASTRI

Mission

To enhance Hong Kong's competitiveness in technology-based industries through applied, innovative research

Research Focuses

CT ECE ICD MPT BME

New initiative: Exploratory Research Laboratory (ERL)

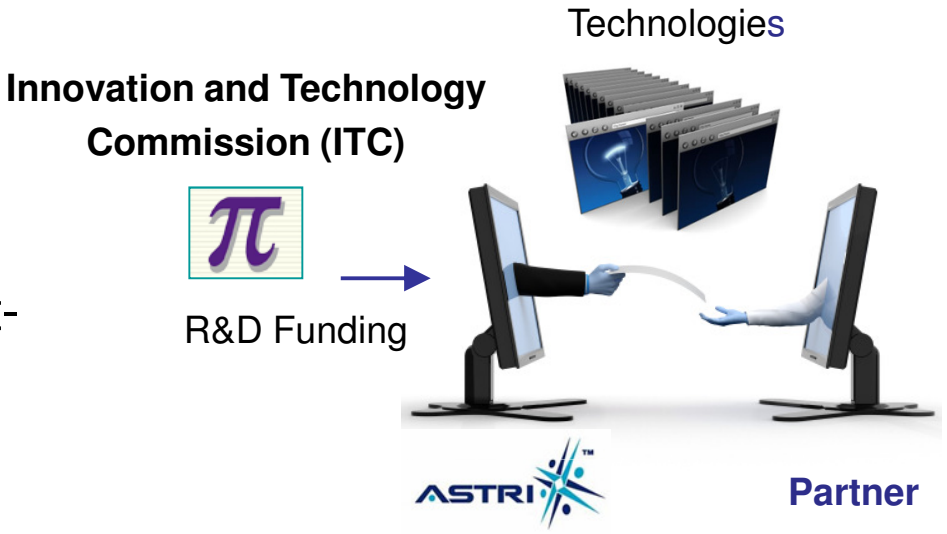
ASTRI Science & Technology Research (Shenzhen) Co. Ltd

- Established in 2008
- ASTRI wholly-owned subsidiary

Competitive Business Models

1) Non-Exclusive Licensing

- Project R&D Resources:
  - Industry Contribution (10%)
  - ITC of HKSAR (90%)
- Industry partner has the right-to-use ASTRI's technology



2) Exclusive Licensing

- Project R&D Resources:
  - Industry Contribution (50%)
  - ITC of HKSAR (50%)
- Industry partner wholly-owns intellectual properties (IPs) created in the project

3) Contract Research

- Project R&D Resources:
  - Industry Contribution (100%)
  - ASTRI's profit margin is very attractive to industry partner

4) Company Spin-off

Technical and Business Achievements

Professional Staff

Total 580

(500 R&Ds, 80 Admins)

Of the R&D Staffs:

- **50% are Master holders**
- **25% are PhD holders**
- **~50% are members of Professional Association**

Patent

Over 200 since inception

Technology Transfer

Close to 400 since established in 2000

Spin-off

4 completed and several underway

Investment made in R&D

292M HKD in 2011

IC Design Group
Applied SoC Design Team

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ASTRI ASD is a team of 42 Members

Average 10+ years SoC design and “First-pass” tapeout experience
Prior employers include:

Technical Excellence: Proven IC Design Flow

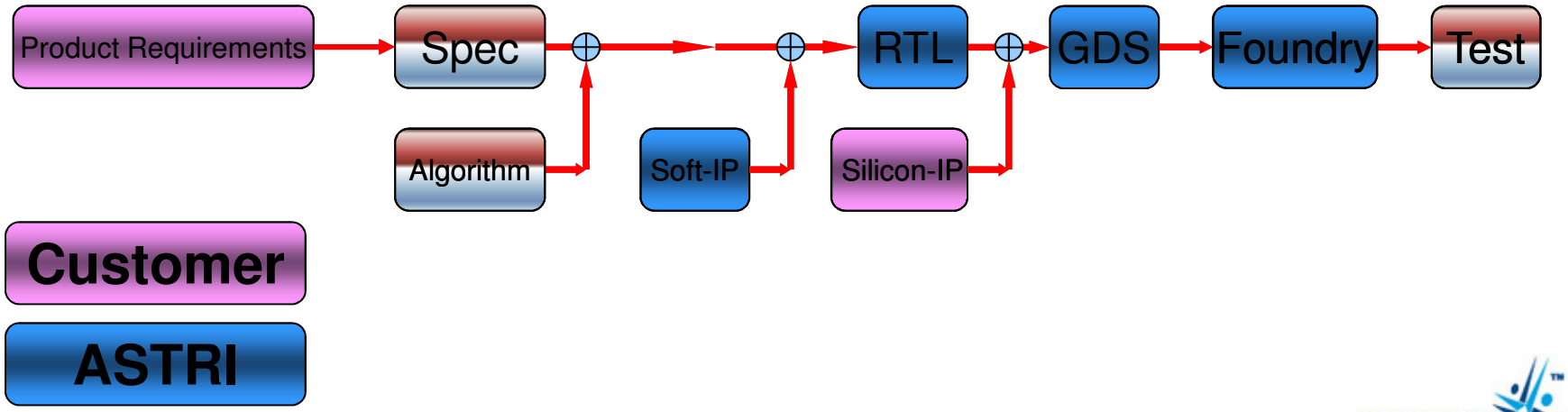
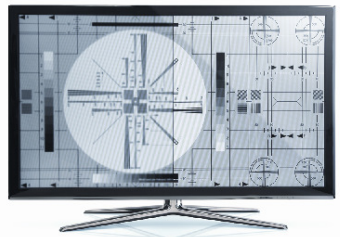


Image Processing Technology Roadmap

Applied SoC Design

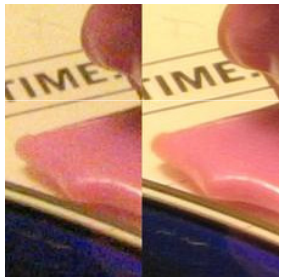
Frame Rate & 2D-3D Converter

3D Surgical



Holography

3D Image Signal Processor



LED Backlight Controller

Super Resolution

Imaging

HOMI (Seed, 6Mo)

LDEC Display Enhance Controller (Full, 21 Mo)

3DHS 3D Holographic System (Seed)

FABC Backlight Controller (Full, 14 Mo)

SISP Stereoscopic Image Sig Processing (Full, 21 Mo)

HAST Hardware Accelerated Super Resolution (Full, 21 Mo)

Keep Innovate…

2008 2009 2010 2011 2012 2013 2014 2015

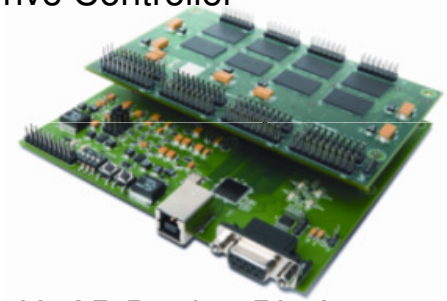
Completed | On-Going | New | Proposals | Plan

Storage Technology Roadmap

Applied SoC Design

SATA Rev 2.0 Solid State Drive Controller

SuperSpeed Solid State Drive Controller



U3AP Design Platform

Storage Server I/O Throughput Accelerator

Storage

HPSC High Performance Storage Controller (Full, 19 Mo)

SCSU SSD Controller with USB3 (Full, 18 Mo)

U3AP USB3 Application Processer (ICP, 19.5 Mo)

EPSA Enterprise PC Based Acceleration Platform (Seed)

Keep Innovate…

2008 2009 2010 2011 2012 2013 2014 2015

Completed | **On-Going** | **New** | **Proposals** | **Plan**

USB 3.0 Application Processor

香港應用科技研究院有限公司
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USB has Changed the World, Electronically

Courtesy of Eltima Software

Universal Serial Bus

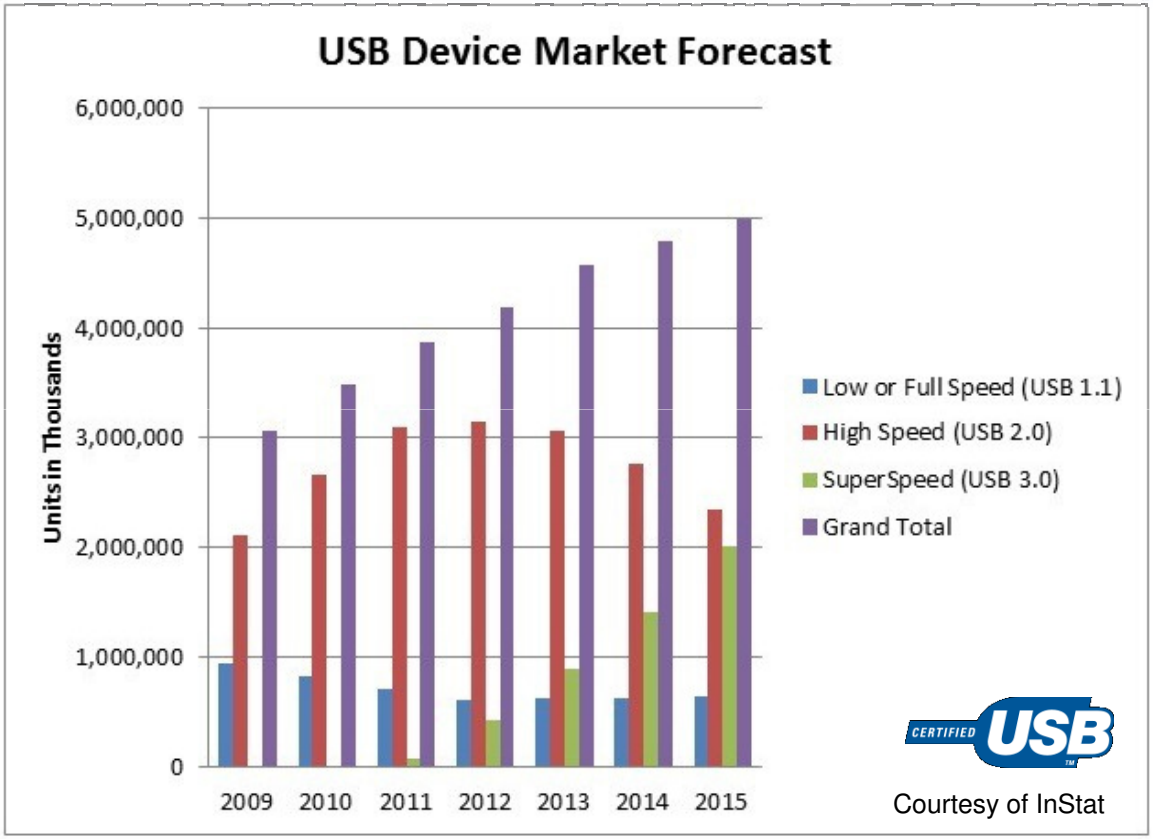
- An industry standard that defines the cables, connectors and communications protocols used in a bus for connection, communication and power supply between computers and electronic devices – Wikipedia
- Exists in Countless Digital Devices
- Brought Convenience to Us All

The New 3.0 Standard

- Max transmission speed of up to **5 Gbit/s (625 MB/s)**
- **10x** as fast as USB 2.0
- Max current of 900mA
- Suspend current of < **2.5mA**
- High data throughput & low power consumption during idle **(Green Technology!)**
- **Backward compatible** with USB 2.0

USB Market Dynamics

2 BILLION USB 3.0 UNITS BY 2015



Why the huge volume?

USB3.0 to be embedded in these **hottest selling** devices

- Smartphones

- Tablets

- Ultrabooks

Start of the USB3.0 Era

- Intel and AMD PC chipset official support in 2012

ASTRI's Successful U3 Mission and Story

Promote Technical Innovation | **Deliver Excellent Design Expertise** | **Maximize Partner's Profit**

Collaboration Project Name:
USB 3.0 Application Processor (U3AP)

Industry Partners:
Velosti
Dr. Patrick Hung, CEO
(Right in Bottom Picture)

ASTRI
Dr Cheung Nim-kwan, CEO
(Top Picture)

Responsible Team:
IC Design Group -
Applied SoC Design Team

Project Coordinator:
Mr. Y. K. Li
(Left in Bottom Picture)

Technical Lead:
Mr. Alan Cheung

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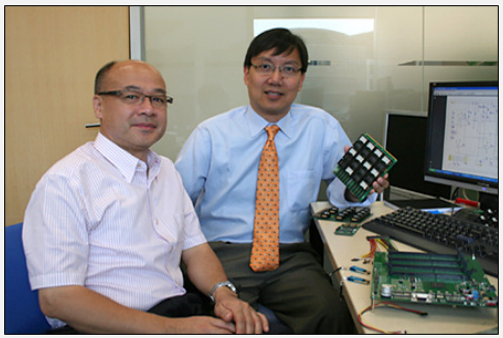
2011 ASTRI Industry and University Consultation Forum (Hong Kong)
ASTRI
2011 ASTRI Industry and University Consultation Forum (Hong Kong)
28.09.2011



Market Values of ASTRI U3AP

ASTRI "Silicon-Proven", Reliable, Low Risk, Total Solution

- Saves customer millions in engineering and capital investment
- Transfers of rare U3 design expertise through technology licensing
- Customizes according to customer's special requirements

High Performance with Niche

- Read 7 times faster and Write 14 times faster than USB2.0 flash drive
- Beat other existing USB3.0 competitors with integrated, hardware encryption

Importance of Security Features

- Based on recent survey of 700+ companies, missing USB sticks represents 70% of all data breaches, costing US$2.5M on average for each company

ASTRI U3AP

Typical U2

Data Encryption

Computer Authentication

Ease of Market Entrance

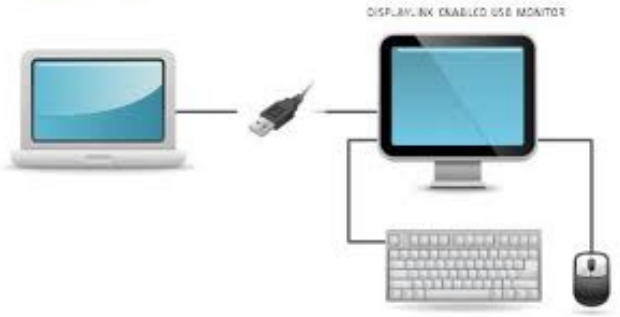
U3AP is a Configurable Design Platform that allows customers to meet Time-to-Market

Besides mobile devices, other applications include:

- U3 Hub

- U3 Thumb Drive

- U3 Display controller



List of Key Intellectual Properties:

- USB 3.0 Upstream Controller
- USB 3.0 Downstream Controller
- SLC/MLC NAND Flash Controller with 30-bit ECC engine
- 32-bit ARM Processor
- AMBA Subsystems
- Display Controller

Configurable SoC Architecture

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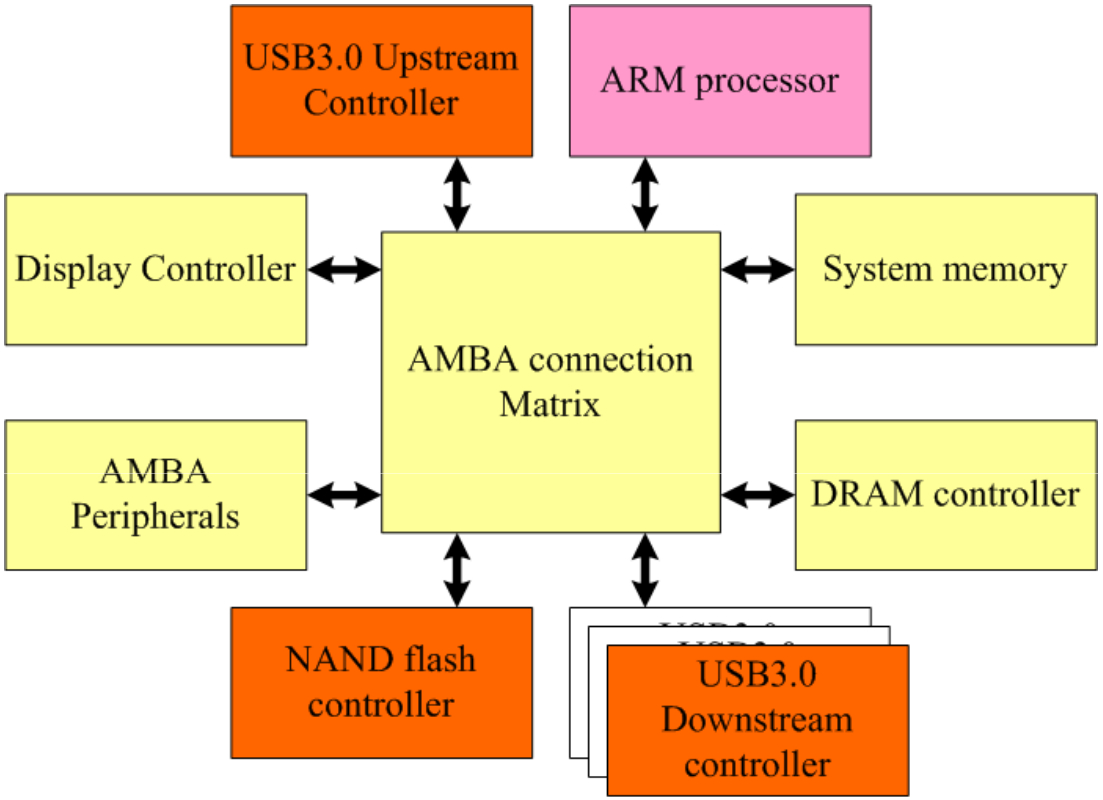
Technical Features of U3AP



Securing Confidentiality

- **XTS-AES 256-bit Strong Encryption**

Energy Efficient, Green Tech

- **Performance acceleration**
  - **Custom connection matrix, RTL engine and USB wrapper**
- **Design optimization for various power saving modes in U3**
- **10mW Standby Power**

Reliable Storage Solution 90nm, ARM7-TDMI, NAND Flash Controller (NFC)

- **Support traditional/ONFI2.x/Toggle Flashes running up to 200MT/s**
- **4kB/8kB pages**
- **Read: 200MB/s max**
- **Write: 130MB/s max**
- **Up to 30bit ECC for MLC/SLC flashes**
- **Advanced wear leveling**
  - **Prolong Flash write reliability**

The Design of U3AP

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ASD SoC Design Flow

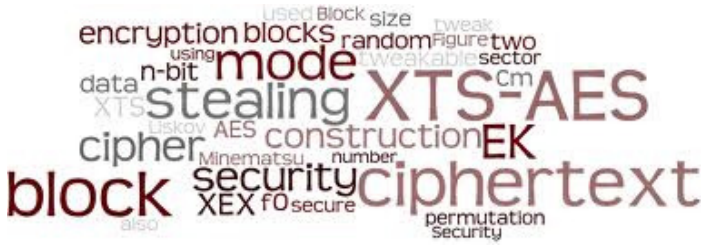
```
always @(posedge clk or negedge rst_n)
 begin : dstatus

 // @@@@
```

Security Algorithm Design

2 Algorithm & Architecture Design

Hardware XTS-AES Engine:

- Compliant to Advanced Encryption Standard as announced in FIPS PUB 197
- Capable to perform encryption and decryption
- Maximum data rate:
  - 10 M bit/MHz using 128 bit key
  - 9 M bit/MHz using 192 bit key
  - 8 M bit/MHz using 256 bit key



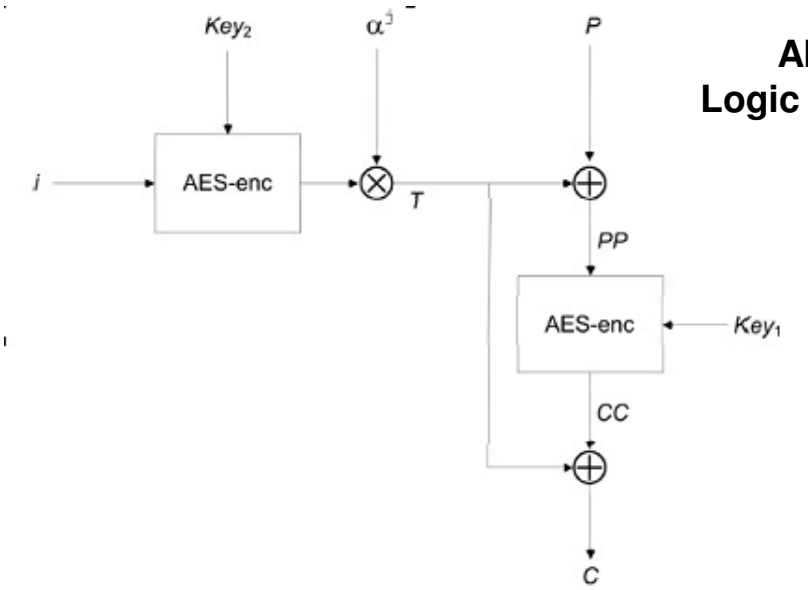
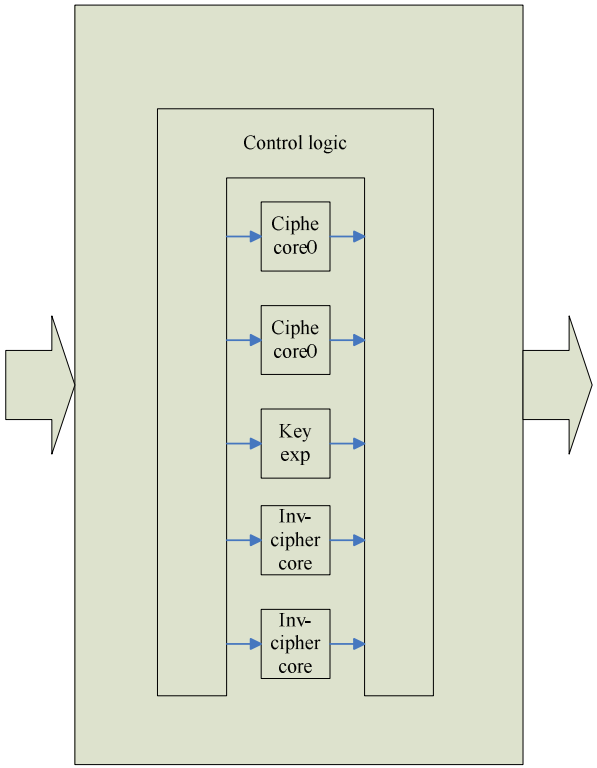


Figure 1— Diagram of XTS-AES blockEnc procedure

Algorithm to Logic Implementation



Two cores AES_XTS architecture

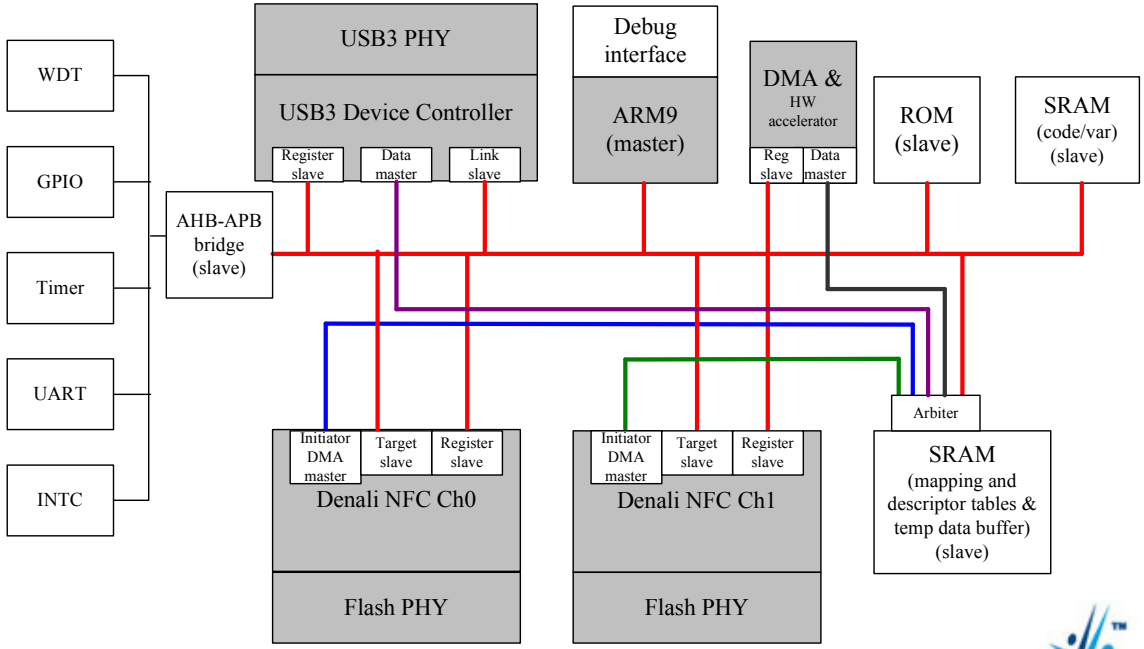
Architecture and Logic Design

2 Algorithm & Architecture Design

3 Firmware / Lgoic Coding

Algorithm defines the absolute performance limit, genuine architecture and logic implementation archives it:

- **Max data throughput:**
  - Design of AMBA Bus Connection Matrix and peripherals
- **Computation performance acceleration:**
  - Build custom logics (e.g. HW accelerator & USB wrapper)
- **Power Efficiency:**
  - Optimize design for low power such as to meet stringent requirement of power saving modes (U1-U3) in USB3.0



Firmware Design

3 Firmware / Lgoic Coding

Firmware is crucial to USB 3.0 host-device compatibility, reliability and product flexibility:

- **Handles USB controller & peripheral initialization, error handling and data flow control**
- **Specific functions per product**
  - Thumb Drive – wear leveling, table swapping etc
  - Hub – U3 Masquerade, U2 Transaction Translation
  - Display – decompression control

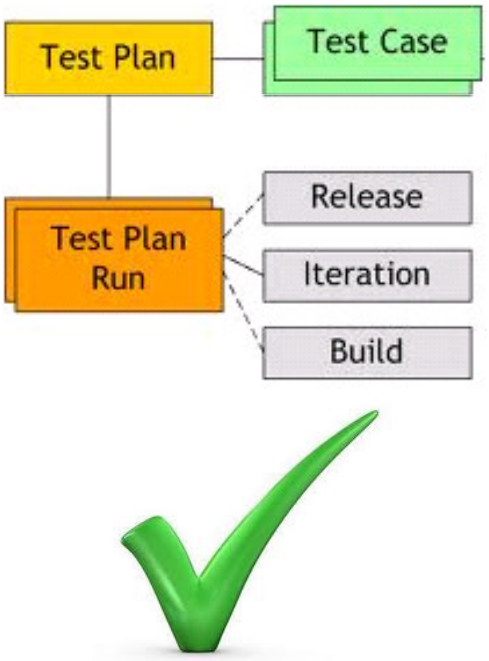
R/W CMD	SCSI CMD	LBA Read	LBA Write	Wear leveling	Garbage Collection	Error Handling	Power Management
FTL		L2P Mapping	Free Block Management	Data Buffer Management	Table Swap		
Data Operation	USB Request (UASP/BOT)	USB Data Transfer Operation		NAND Operation R/W/Erase	Table Update Operation		
Driver	USB IF Driver		NFC Driver		ISR		
Hardware	USB IF	NAND IF		ARM7	SRAM	Boot Loader	

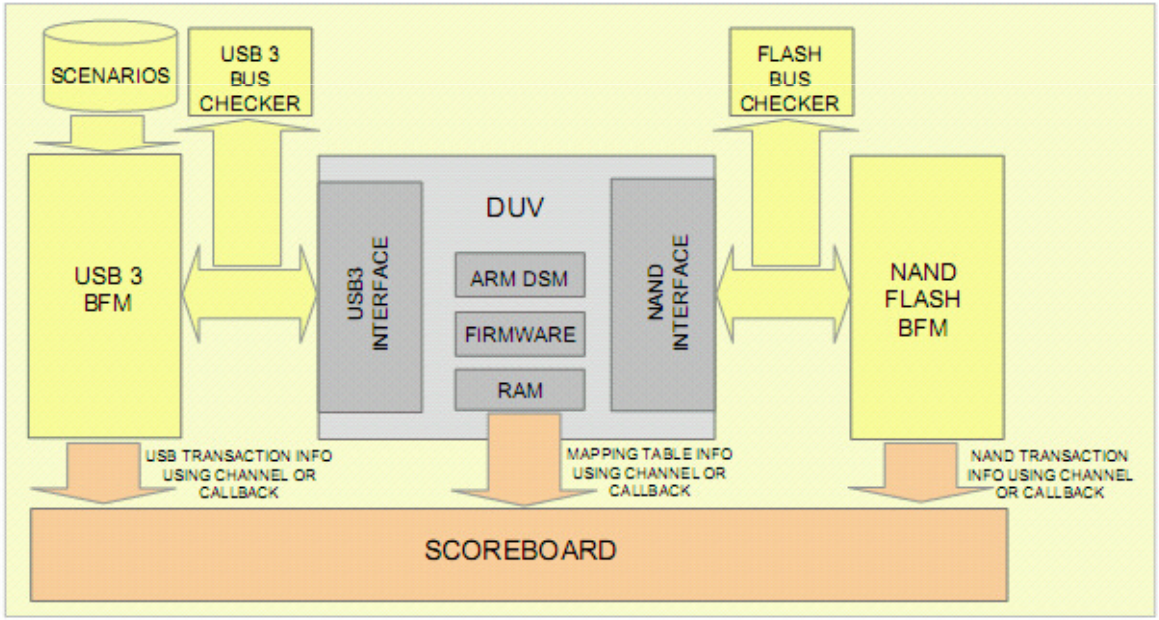
Logic Design Verification

4
Verification & Code Coverage

Carefully planed verification ensures the correctness of logic behavior:

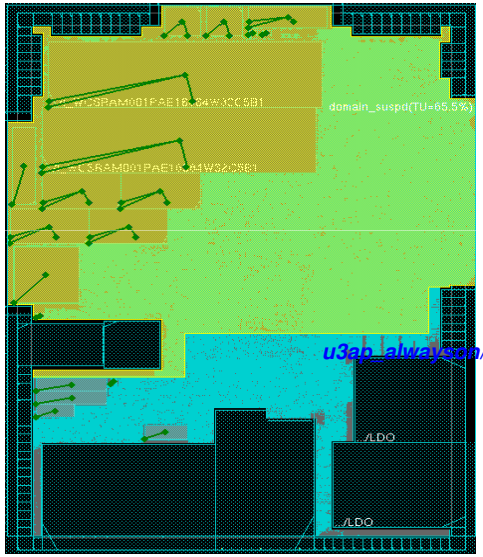
- **Build system verification environment with all behavioral models and checkers (e.g. USB3.0 Host & NAND Flash model)**
- **Design complete test plan documentation and extensive test cases to ensure maximum functional and code coverage**
- **Make use of off-the-shelf verification IPs (Synopsys & Denali) to speed up verification time**

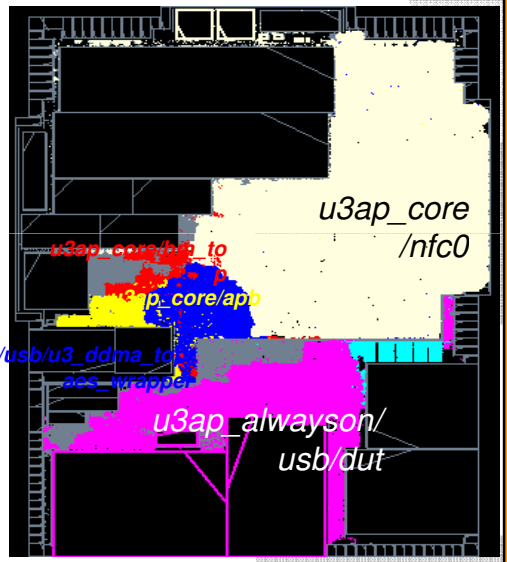


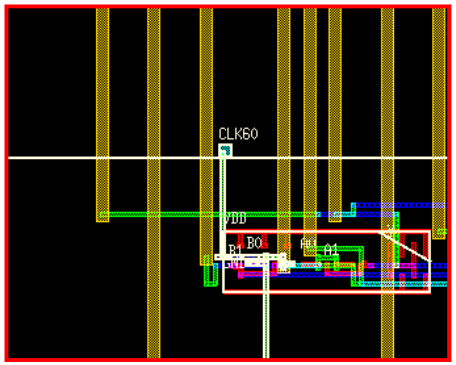


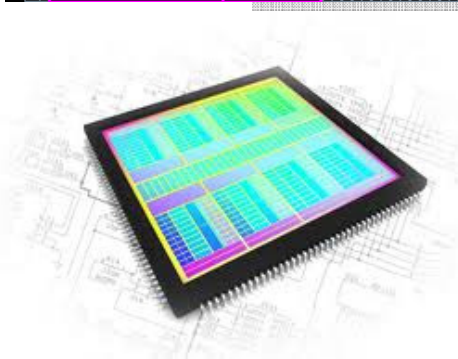
Physical Design

Squeezing the last drop of power efficiency and timing requirement with state-of-the-art techniques









Timing Closure	SI Closure	Area Optimization	Power Optimization
	RTL Synthesis w/ Clock Gating, Multiple Power Domains		Synthesis & DFT
	Dynamic and Leakage Power Optimization		
	DFT		
	Multi-Supply-Voltage (MSV) Floorplanning		Floorplanning
	MSV Power Planning and Optimization		
	Placement and Level Shifter/Power Switch Insertion		Placement, Clock Tree, Optimization
	Multi-Vth / MSV Power-aware Clock Tree Synthesis		
	Multi-Vth / MSV-aware Timing Optimization		
	MSV-aware Power Routing		Routing, Optimization
	Timing & SI Driven, MSV-aware Signal Routing		
	Post-route Timing & Power Optimization		
	3-D RC Extraction		Signoff Verification
	MSV-aware Timing Analysis		
	MSV-aware Xtalk Analysis		
	Low Power Formal Verification		
	Static & Dynamic Power Rail & EM Verification		
	Physical Verification		

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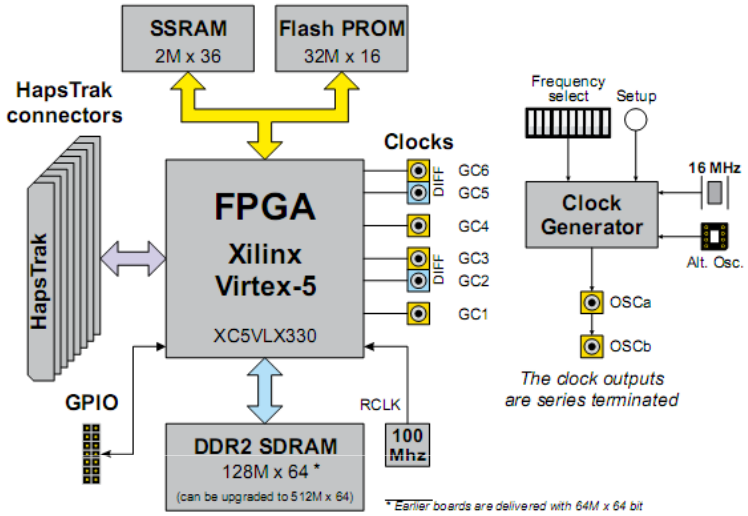
Prototype and Physical System Bring Up

FPGA prototype to serve as further firmware development and test bed:

- Build a versatile board that connects with ARM CPU core and USB3.0 PHY ICs
- FPGA board can be easily extended for future USB3.0 applications development

5
FPGA
or
Structure ASIC



Testchip physical system is the closest to the final product

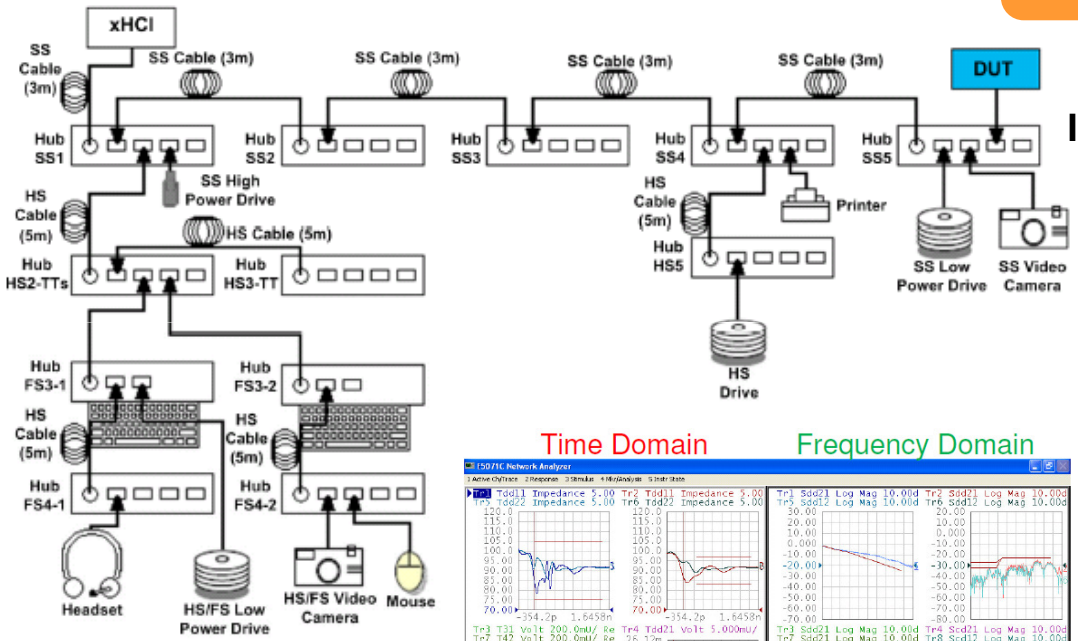
- The final performance measures are realistic, or physical
- Firmware designers can perform software tuning for the SoC chip running at real speed

8
System
Hardware
Bring up

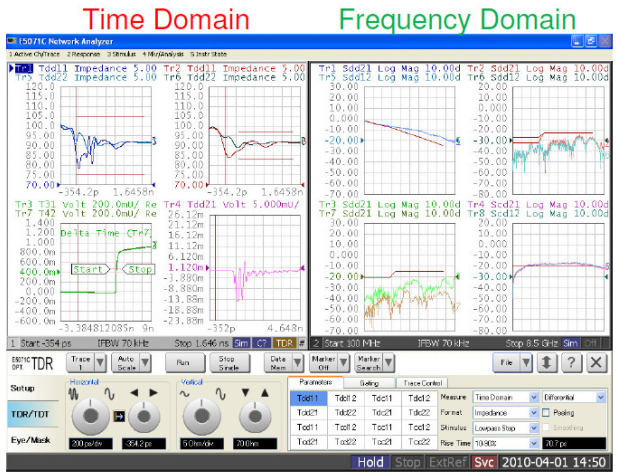
USB 3.0 Compliance Tests and Certification

Last but not least, the final challenge of countless testing:

9 Pre-Production Testing



Example: Testing Environment



Example: Testing Measurements

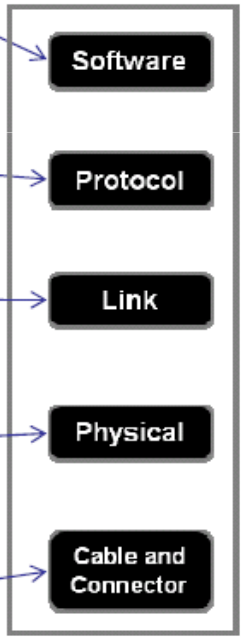
Framework and Interoperability Testing

Protocol Testing

Link Testing

Electrical Testing

Cable and Connector Testing



ASTRI Storage Design Platform

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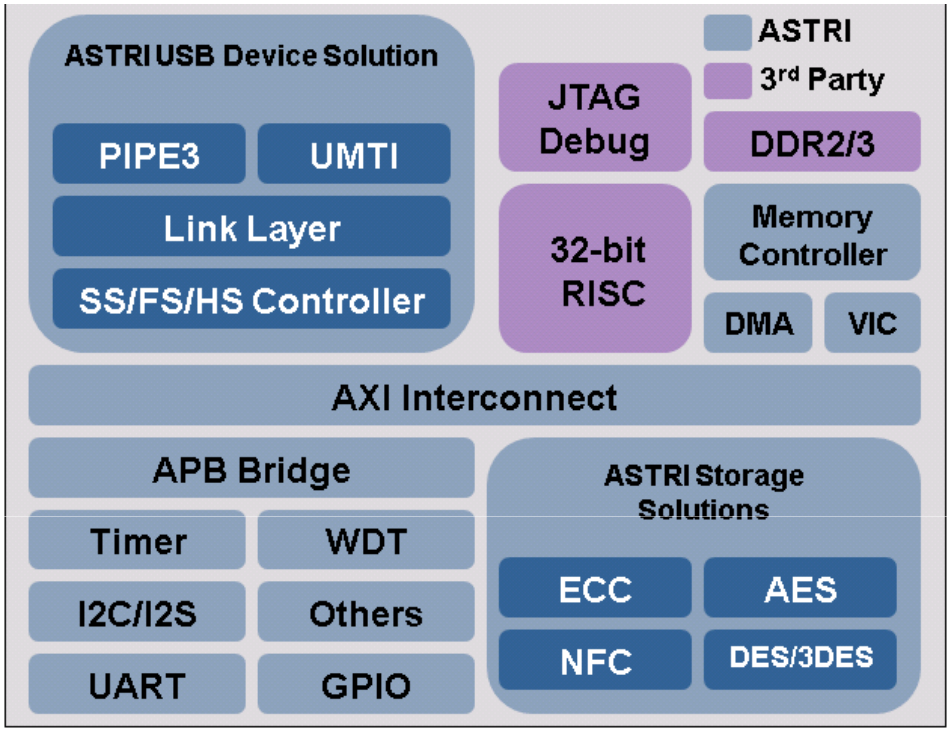
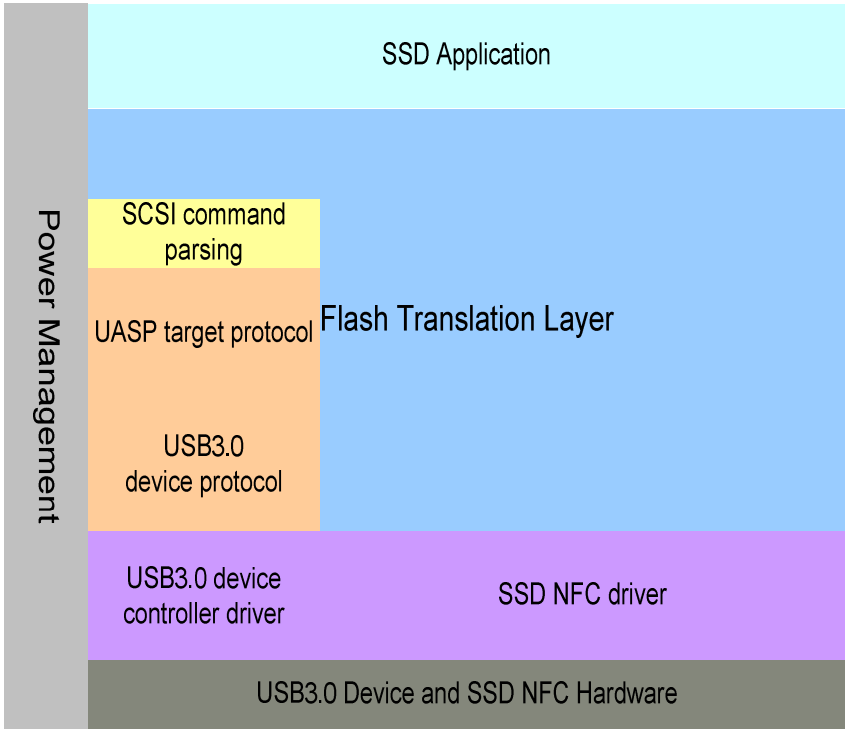
Hong Kong Applied Science and Technology Research Institute Company Limited

Secure and Configurable





Based on Silicon-Proven Experiences

1. Hardware design platform that has built-in *hardware accelerated security* and can be easily integrated with other *high throughput interfaces*
2. Reference firmware library that further *reduces design time and cost*
3. ASTRI's *world-class expertise* on ASIC and system verification and testing

New Project Preliminary Specificatic

Available in Q3 2012

Hardware

General
•Process: 90nm
•System Frequency:240Mhz
•Package: BGA209
•IO Voltage: 3.3/2.5/1.8V
•Core Voltage: 1.0V

CPU and Subsystem
•32-bit ARM 9
•AXI bus architecture

Memory
On-chip
•SRAM: 232KB
•ROM: 16KB
Off chip
•DDR2: up to 512MB

Interface
•USB3.0 SuperSpeed
•Customizable to SATA 3Gbps/6Gbps, PCIe etc. at client's request

NAND Flash Controller
•Up to 4 channels of ONFI2.2 synchronous interface
•Up to 32CEs
•BCH ECC up to 72 bit in 1K Byte data
•Support 2K/4K/8K/16K bytes page size

Target Performance:
Read: 400MB/s
Write: 320MB/s

Firmware

•Support UAS (USB Attached SCSI) protocol
•Fully compliant with USB3.0 super speed specification
•Support SPC-4 command queuing
•Optimal read/write strategy for SLC/MLC
•Enhanced endurance by dynamic/static wear-leveling
•Supports dynamic power management
•Supports SMART (Self-Monitoring, Analysis and Reporting Technology),
•Data integrity under power interrupts
•Efficient logic to physical page/block mapping

End of Presentation

Thank you. Questions are welcome.

Our corporate website: www.astri.org

Successful Spin-off Cases

2010: AP Photonics Ltd.

A world leader in the design, development and production of optical and opto-mechanical products

Established by a group of scientists and engineers spinning off from ASTRI. The company licensed 8 ASTRI patents for smart phone cameras and has started production in Shenzhen

2006: Altai Technologies

A high technology company focused on the design, development and marketing of carrier-grade, innovative wireless broadband solutions

Incorporated in 2006 after licensing ASTRI technologies in an exclusive manner. Within 6 months after the licensing, Altai closed its Series A equity financing with a total amount of US$10M

2005: Marvell Technology Group Ltd - R&D Centre

A leading fabless semiconductor company, Marvell ships over one billion chips a year. High Performance with Niche

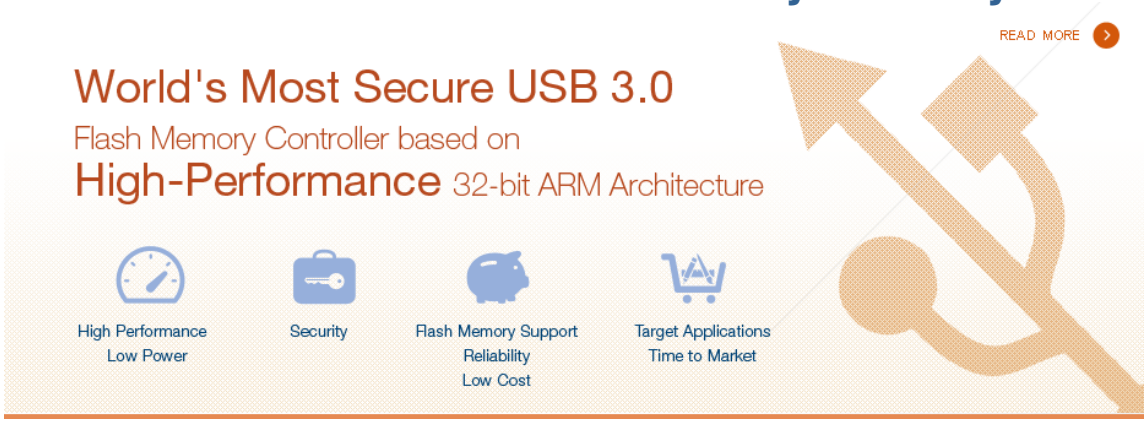
An international semiconductor company, set up an R&D centre in Hong Kong after acquiring ASTRI's technologies. The core team of the R&D centre was mainly from ASTRI

2004: ASTRI's Photonic Technologies - SAE Magnetics

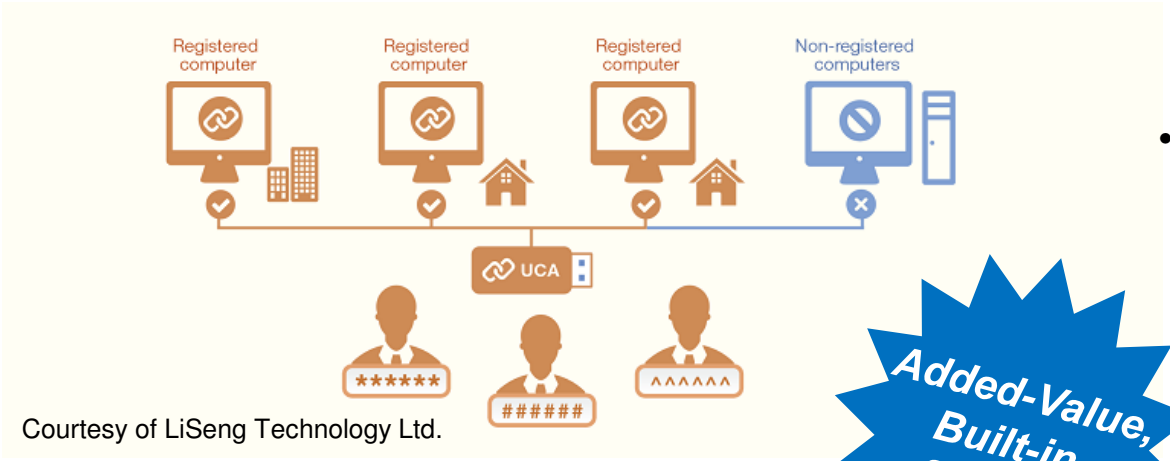
ASTRI's photonic technologies and related assets were sold to SAE Magnetics (HK) Ltd at HK$109M plus 3 years' royalty. Within 2 years, ASTRI successfully spun off the projects which were funded by ITF at around $40M. Seventeen ASTRI staff joined the new company

Competitive Differentiation

Unlike Traditional Password-only Security Solutions



Innovative User-to-Computer Authentication



Courtesy of LiSeng Technology Ltd.

Added-Value, Built-in Security

UCA (User-Computer-Authentication) security algorithm:

- Does not depend strictly on your password strength
- Supports concurrent user and computer authentication
- Authorized users can only access their sensitive data in registered computers
- All storage data are encrypted using an AES cipher key, which can only be calculated using authorized user passwords and registered computer signatures